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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/697,305	10/27/2000	Takaki Yoshida	YMOR:186	4222

7590 11/29/2004

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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 11/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/697,305	YOSHIDA ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) *23-52 and 54-58* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-18,20-22 and 53* is/are rejected.

7)☒ Claim(s) *8 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. This application contains claims 23-52 drawn to an invention nonelected with traverse in Paper No. 6. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Newly submitted claims 54-58 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-22 and 53, drawn to Fault Detection by providing a fault list corresponding to (a) information identifying physical sites on a physical layout of a semiconductor integrated circuit where a possible fault is likely to occur, and (b) information required to reduce faults; and detecting faults in a semiconductor integrated circuit to which said fault list corresponds, classified in class 714, subclass 724.

II. Claims 23-52, drawn to Circuit Design and Floorplanning, classified in class 716, subclass 8.

III. Claims 54-58, drawn to Fault Detection by limiting one of a type of fault and a position of fault on the basis of a detection change resulting from a change of a detection condition, classified in class 714, subclass 811.

The inventions are distinct, each from the other because of the following reasons:

The inventions are distinct, each from the other because of the following reasons:

Inventions Group I, Fault Detection, and Group II, Circuit Design and Floorplanning, are unrelated. Inventions are unrelated if it can be shown that they are not disclosed as capable of use together and they have different modes of operation, different functions, or different effects (MPEP § 806.04, MPEP § 808.01). In the instant case the different inventions Fault Detection occurs on actual circuits after manufacture of the circuit and cannot occur before whereas Circuit Design and Floorplanning occurs before the circuit is manufactured. Since Fault Detection and Floorplanning occur at different mutually exclusive times during the circuit life cycle it is not possible to use the two inventions together.

Inventions Group I and Group III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group I has separate utility such as for providing a fault list corresponding to (a) information identifying physical sites on a physical layout of a semiconductor integrated circuit where a possible fault is likely to occur, and (b) information required to reduce faults; and detecting faults in a semiconductor integrated circuit to which said fault list corresponds. In the instant case, invention Group III has separate utility such as for limiting one of a type of fault and a position of fault on the basis of a detection change resulting from a change of a detection condition. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group II is not required for Group I, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group III, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group III is not required for Group I, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

Since applicant has received an action on the merits for the originally presented invention of claims 1-22, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 23-52 and 54-58 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Objections

2. In view of the amendment filed 08/26/2004, the Examiner withdraws all objections to the claims.

Claim Rejections - 35 USC § 102

3. In view of the amendment filed 08/26/2004, the Examiner withdraws all previous ***35 USC § 102*** rejections to the claims.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 54-58 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. cMPEP 2164.08(a) states, "A single means claim, i.e., where a means recitation does not appear in combination with another recited element of means, is subject to an undue breadth rejection under 35 U.S.C. 112, first paragraph. In re Hyatt, 708 F.2d 712, 714-715, 218 USPQ 195, 197 (Fed. Cir. 1983) (A single means claim which covered every conceivable means for achieving the stated purpose was held nonenabling for the scope of the claim because the specification disclosed at most only those means known to the inventor.)." Claims 54-58 are single means claims.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 54-58 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 54-58 recite, "A fault detecting method for a semiconductor integrated circuit" in the preamble, but the body of the claims do not have any tangible step for detecting a fault on a semiconductor integrated circuit.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 54-58 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The body of claims 54-58 recites an abstract step that has no tangible connection to any useful process, machine, manufacture, or composition of matter.

Response to Arguments

7. Applicant's arguments filed 08/26/2004 have been fully considered but they are not persuasive.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "However, the Balachandran '830 stuck-at-fault directory does not include physical layout information identifying physical sites on a physical layout of a semiconductor integrated circuit where a possible fault is likely to occur, as recited in applicants' claim 1") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Claim 1 does **not** recite anywhere in the claim that "the fault list" includes "information identifying physical

sites on a physical layout of a semiconductor integrated circuit where a possible fault is likely to occur". Claim 1 recites, "a fault list corresponding to information identifying physical sites on a physical layout of a semiconductor integrated circuit where a possible fault is likely to occur". The Applicant admits Balachandran "describes physical layout information coming from other sources within the overall system" corresponding to faults.

The Applicant contends, "regarding claim 9, applicants submit that the Office Action is not correct in alleging that detecting defects is a step for using functional blocks in an IC, hence the reliability data is based on past use. There is no basis in the record for supporting such conclusion".

The Examiner disagrees and asserts that col. 3, lines 56-67 and col.4, lines 1-6 in Balachandran teach that the step for detecting faults includes the steps of generating test patterns, using scan circuitry to apply the test patterns to functional blocks in the semiconductor integrated circuit and comparing results to expected values; hence detecting defects is a step for using and exercising functional blocks in an IC to verify the integrity or the lack thereof of the functional blocks.

The Applicant contends, "None of Balachandran '830, Rohrbaugh '651 or Agrawal '268 discloses or suggests deletion of possible fault coverage to satisfy a special fault coverage, as recited in applicants' claims 10 and 21."

The Examiner disagrees and asserts that col. 2, lines 43-48 in Balachandran teaches omitting possible faults that having a specified low probability of occurrence from the fault list to define a remaining part of the fault list.

The Examiner disagrees with the applicant and maintains all rejections of claims 1-22. All amendments and arguments by the applicant have been considered. It is the Examiner's conclusion that claims 1-22 are not patentably distinct or non-obvious over the prior art of record in view of the references, Balachandran; Hari et al. (US 6618830 B1, hereafter referred to as Balachandran), Rohrbaugh, John G. et al. (US 6067651 A, hereafter referred to as Rohrbaugh), Allan; Gerard Anthony (US 6066179 A) and Agrawal; Prathima et al. (US 5257268 A, hereafter referred to as Agrawal)as applied in the last office action, filed 05/26/2004. Therefore, the rejection is maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1 and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by Balachandran; Hari et al. (US 6618830 B1, hereafter referred to as Balachandran).

See the Non-Final Action filed 05/26/2004 for detailed action of prior rejections.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 2, 4-6, 9, 12-17, 20 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balachandran; Hari et al. (US 6618830 B1, hereafter referred to as Balachandran) in view of Rohrbaugh, John G. et al. (US 6067651 A, hereafter referred to as Rohrbaugh).

See the Non-Final Action filed 05/26/2004 for detailed action of prior rejections.

35 U.S.C. 103(a) rejection of claim 53.

Balachandran substantially teaches the claimed invention described in claims 1-3 (as rejected above). In addition, Balachandran teaches weighting possible faults at physical

sites according to their likelihood to achieve a specific fault coverage, thereby creating weighted possible faults (col. 6, lines 31-44 in Balachandran teach that if such a defect can cause a bridging fault between the two particular nets, the determination is weighted using the probability that a defect of that size exists to determine a final probability or ranking that particular bridging fault exists, hence ranking is a means for weighting in the Balachandran patent). Note: fault coverage is a probabilistic measure of detecting a set of faults in a semiconductor integrated circuit using a particular fault list.

Col. 5, lines 22-42 in Balachandran teach that a composite dictionary including a listing of faults is used to create the final logical diagnostic list. A listing is an ordered set, i.e., the composite dictionary is ordered; hence Balachandran teaches arranging said possible faults an order in a composite dictionary before weighting said possible faults in the final logical diagnostic list.

However Balachandran does not explicitly teach the specific use of detecting faults in said semiconductor integrated circuit by using the remaining part of the fault list. Rohrbaugh, in an analogous art, teaches the typical use of fault lists for compacting test vectors (see Figure 7 in Rohrbaugh). The Examiner asserts that Balachandran teaches a method for creating a pruned fault list, which are typically used and required for designing tests, for creating test pattern sets and for testing for faults in Automatic Test Equipment (ATE) throughout the lifecycle of the DUT. Rohrbaugh, on the other hand teaches a typical use for generating test patterns from a fault list (see Figure 7 in Rohrbaugh) and using generated test patterns for testing a Device Under Test (DUT) by

detecting faults using test patterns that were generated using a fault list, hence Rohrbaugh teaches detecting faults in said semiconductor integrated circuit by using the remaining part of the fault list.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Balachandran with the teachings of Rohrbaugh by including an additional step of detecting faults in said semiconductor integrated circuit by using the remaining part of the fault list. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that detecting faults in said semiconductor integrated circuit by using the remaining part of the fault list would have provided the opportunity to determine the integrity and fault-tolerance of a particular DUT during and after manufacture throughout the lifecycle of the DUT. Note: fault coverage is a probability of detecting faults in said a semiconductor integrated circuit using a particular fault list.

10. Claims 7 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balachandran; Hari et al. (US 6618830 B1, hereafter referred to as Balachandran) and Rohrbaugh, John G. et al. (US 6067651 A, hereafter referred to as Rohrbaugh) in view of Allan; Gerard Anthony (US 6066179 A).

See the Non-Final Action filed 05/26/2004 for detailed action of prior rejections.

11. Claims 10, 11, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balachandran; Hari et al. (US 6618830 B1, hereafter referred to as Balachandran) and Rohrbaugh, John G. et al. (US 6067651 A, hereafter referred to as Rohrbaugh) in view of Agrawal; Prathima et al. (US 5257268 A, hereafter referred to as Agrawal).

See the Non-Final Action filed 05/26/2004 for detailed action of prior rejections.

Allowable Subject Matter

12. Claims 8 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

See the Non-Final Action filed 05/26/2004 for detailed action of prior rejections.

Conclusion

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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